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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/320,271	05/27/1999	HIROYUKI WATANABE	990559	4409

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EXAMINER

LEE, CALVIN

ART UNIT PAPER NUMBER

2825

DATE MAILED: 05/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/320,271

Applicant(s)

WATANABE ET AL.

Examiner

Lee Calvin

Art Unit

2825

-- The MAILING DATE of this communication appears on the cover sheet with the corresponding address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 April 2003 (RCE).
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☐ Claim(s) 1-13, 21 and 22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☐ Claim(s) 1-13, 21 and 22 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 May 1999 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s) _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

OFFICE ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in a patent granted on an application for patent by another filed in the US before the invention by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. Claims 1, 2, and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by *Wada et al* (US 6,071,810).

Wada discloses a method of a semiconductor device formed by Damascene, comprising:

- introducing impurities into a first insulation layer 183 formed on a substrate [Fig. 49B, col 101]
- forming a trench in the first insulation layer [Fig. 28A]
- embedding in the trench a first conductive layer 187 [Fig. 49C]
- forming a second insulation layer 32 on the first insulation layer 31 [Fig. 28D]
- forming a contact hole in the second insulation layer [col. 77]
- forming a second conductive layer in the contact hole, electrically connected to the first conductive layer [Fig. 28E]

Wada also suggests using masks 21a and 21b to form, respectively, contact hole 5 and trench 4, [Figs. 16C-16E]

3. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by *Gambino et al* (US 6,136,686).

Gambino discloses a method of a semiconductor device done by Damascene, comprising:

- introducing impurities into a first insulation layer 22 formed on a substrate 12 [Fig. 5 and col 5]
- embedding and forming in the first insulation layer a first conductive layer 60 62 64 [Fig. 6]

Claim Rejections - 35 U.S.C. § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1, 2, 4, 7-12, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Hsieh et al* (US 5,960,321) in view of *Wada et al* or *Jain et al* (US 6,153,519).

a) In re claims 1 and 10, *Hsieh* discloses a method of a semiconductor device, comprising:

- introducing impurities into a first insulation layer 26 formed on a substrate 20 [Fig. 2B]
- embedding and forming in the first insulation layer a first conductive layer [cols. 1-2]

Hsieh does not suggest using Damascene to form the first conductive layer. *Jain* teaches forming first and second conductive layers 36 66 by Damascene method.

It would have been obvious to one of ordinary skill to have modified *Hsieh*'s process by utilizing Damascene method because Damascene method is notoriously well known as seen by the plethora of *Gambino* [col. 2] and *Jain* both suggesting damascene processes in interconnect.

b) In re claim 2 and 21, *Hsieh* is silent about second, third insulation layers and second, third conductive layers. Nevertheless, such multi-level interconnect structure is known in the semiconductor processing art as evidenced ** by *Jain* disclosing:

- forming a first insulating layer 26 on a flat surface of a substrate 10 [col. 4, lns. 48-61]
 - forming a trench and a contact hole 28 in the first insulating layer by etching [Fig. 1]
 - embedding and forming a first conductive layer 36 in the first insulating layer [col. 5]
 - forming a second insulating layer 56 on a flat surface of the first insulating layer [Fig. 5]
 - forming a trench 52 in the second insulating layer by etching [col. 5, ln. 31]
 - embedding and forming in the second insulating layer a second conductive layer 66 electrically connected to the first conductive layer [Fig. 6]
 - forming other conductive layers in other insulating layers [col. 5, ln. 49]
- ** and by *Wada* disclosing [Figs. 1B] a first conductive layer 82 in a first insulation layer 81, a second conductive layer 83 in a second insulation layer 81, and a third conductive layer 83 in a third insulation layer 81 [cols. 1 and 4]

It would have been obvious to one of ordinary skill to have modified *Hsieh*'s process by utilizing a multilayer structure of interconnection because the multilayer structure is required for complex circuit design.

c) In re claims 4 and 11-12, since *Wada* suggests using a mask 21a and 21b to form a contact hole 5 and trench 4, respectively [Figs. 16C-16E], *Wada* inherently teaches etching first, second, and third insulation layers, using mask patterns, to form first, second, and third openings/trenches, respectively for first, second, and third interconnections.

6. Claims 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Wada et al*, *Gambino et al*, and *Hsieh et al* and *Jain et al*, as applied to claim 1, in view of *Ohbayashi et al* (US 5,863,702).

None of the cited references teaches or suggests the insulating layers comprising silicon oxide containing at least 1% of carbon. *Ohbayashi* teaches dielectric layers, for protecting a semiconductor substrate, comprising inorganic thin films of ZnS, SiO, ... oxide film of a metal such as Si, Ge, ... contain 1 to 15 mol % of carbon [col. 10].

It would have been obvious to one of ordinary skill to have modified the insulating layers of *Jain* by utilizing SiO containing at least 1% of carbon, taught by *Ohbayashi*, because the resulted insulating/dielectric layers can withstand heat and stress.

Allowable Subject Matter

7. Claim 22 is allowed.

8. Claims 3, 5-6, and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims because none of the cited references teaches or suggests introducing impurities into second and/or third insulation layers, and an interface between a first insulation layer and a fourth insulation layer.

Any inquiry concerning this communication from the Examiner should be directed to *Calvin Lee* at (703) 306-5854 from 7 to 17 ET (Monday through Thursday). If attempts to reach the examiner by telephone are unsuccessful, Art Unit 2825's Supervisory Patent Examiner *Matthew Smith* can be reached at (703) 308-1323.

Any inquiry relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0596. The fax phones are (703) 872-9318 for regular communications and (703) 872-9319 for After-Final communications.

CL

C. Lee
CALVIN LEE
PATENT EXAMINER

May 10, 2003